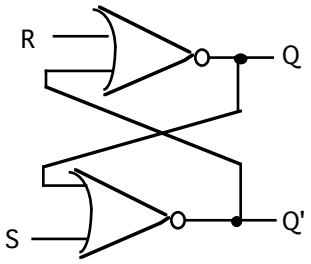
CS240 Laboratory 4
Sequential Circuits

Basic Memory Circuits

Latch Single-bit memory, level-triggered
Flip-Flop Also single-bit, but edge-triggered

SR (Set Reset) Latch



S	R	Q	Q′
0	0	Qp	Qp′ remember
0	1	0	reset (clear)
1	0	1	set
1	1	unpredictable	

SR latch uses 2 cross-coupled NOR gates:

A	B	(A+B)′
0	0	1
0	1	0
1	0	0
1	1	0

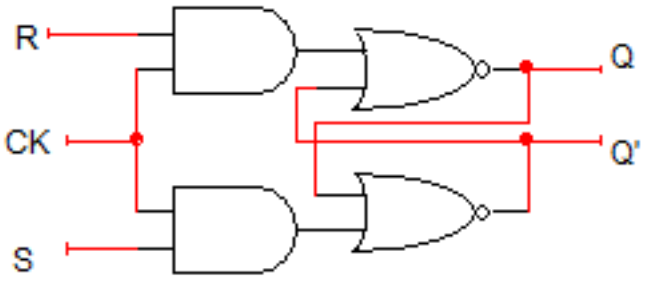
What does **unpredictable** mean? Notice in a NOR gate, if either input = 1 to a gate, its output = 0 (1 is a deterministic input)

You wouldn't usually try to set and reset at the same time (it doesn't make sense), but if you did, Q and Q′ will both be 0.

However, when you go back to the remember state (S=R=0), Q and Q′ will not stay at 0 0. The circuit passes through one of either the set or reset state on its way back to the remember state, and Q and Q' change to the complement of one another.

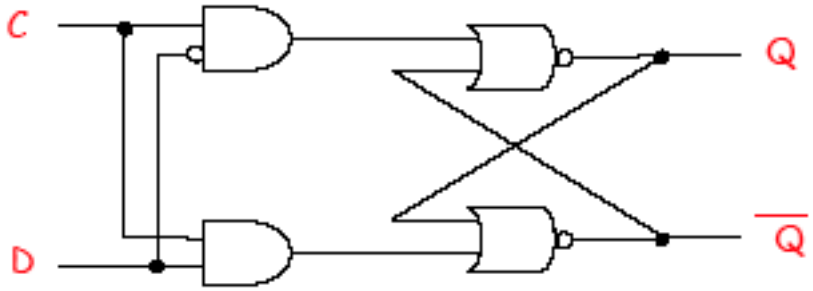
You cannot predict whether Q will be 1 or 0. The final state depends on which transitional state was sensed on the way back to remember.

Clocked SR Latch incorporates a clock input/level-sensitive



Output Q can change in response to S and R whenever the CK input is asserted.

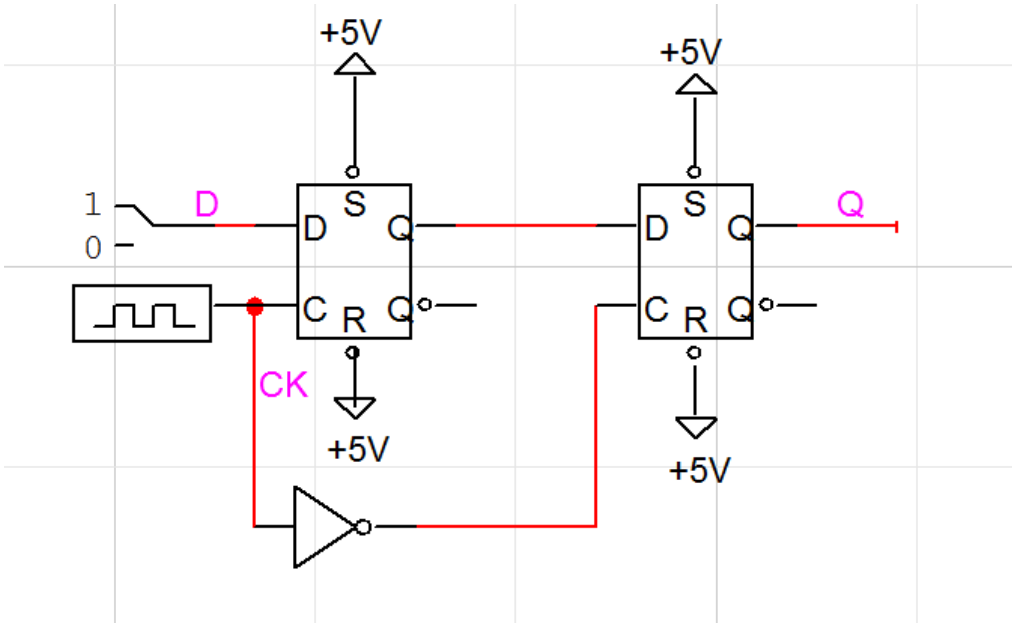
D Latch (avoids unpredictable state)



D	Qnext
0	0
1	1

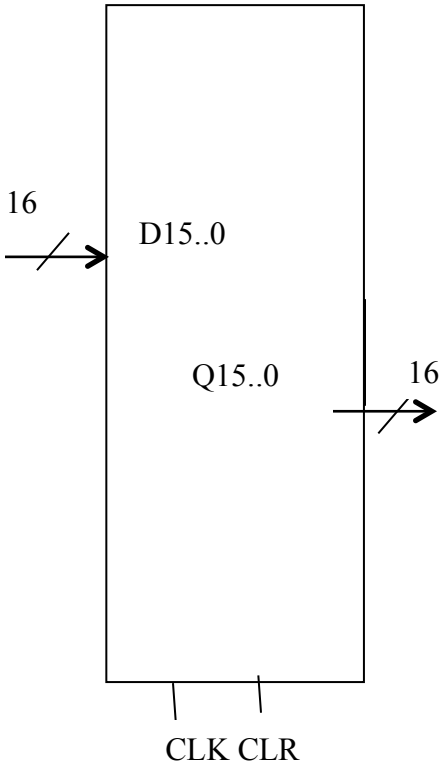
D Flip-Flop edge-sensitive

Output Q will only change value in response to D on the edge/transition of CK from high to low

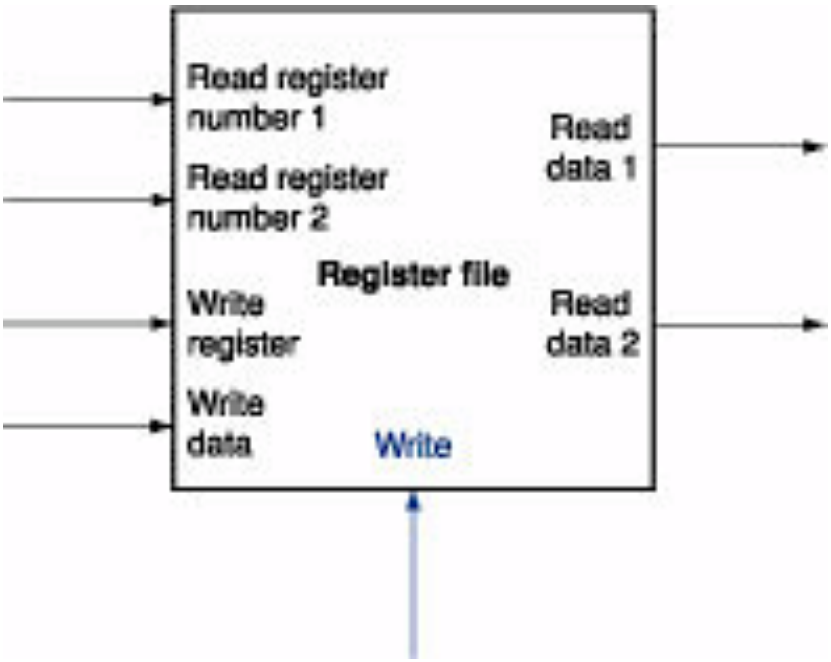


Circuits using Flip-flops

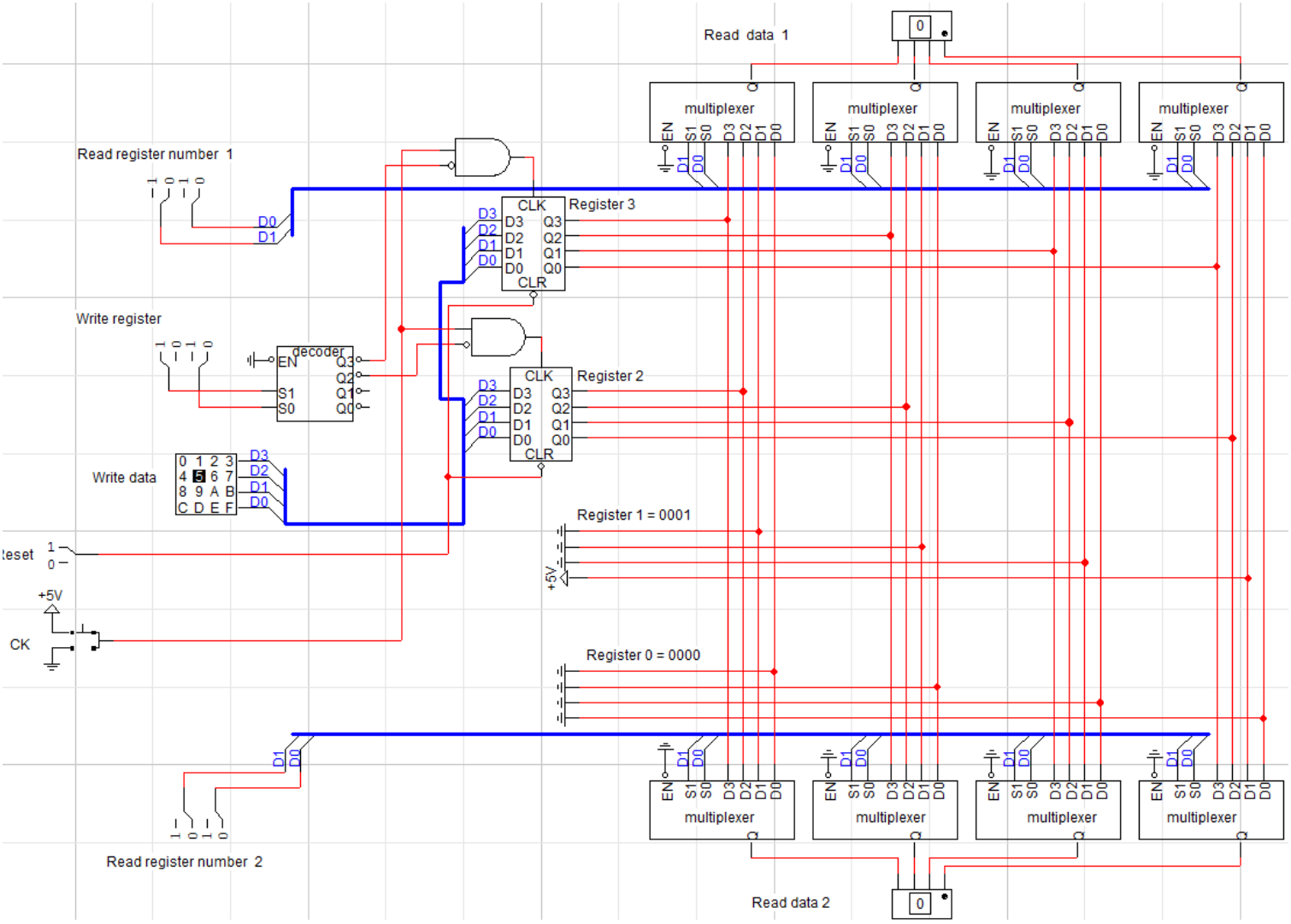
Register n-bit memory, using n flip-flops, shared clock and clear inputs



Register File set of registers



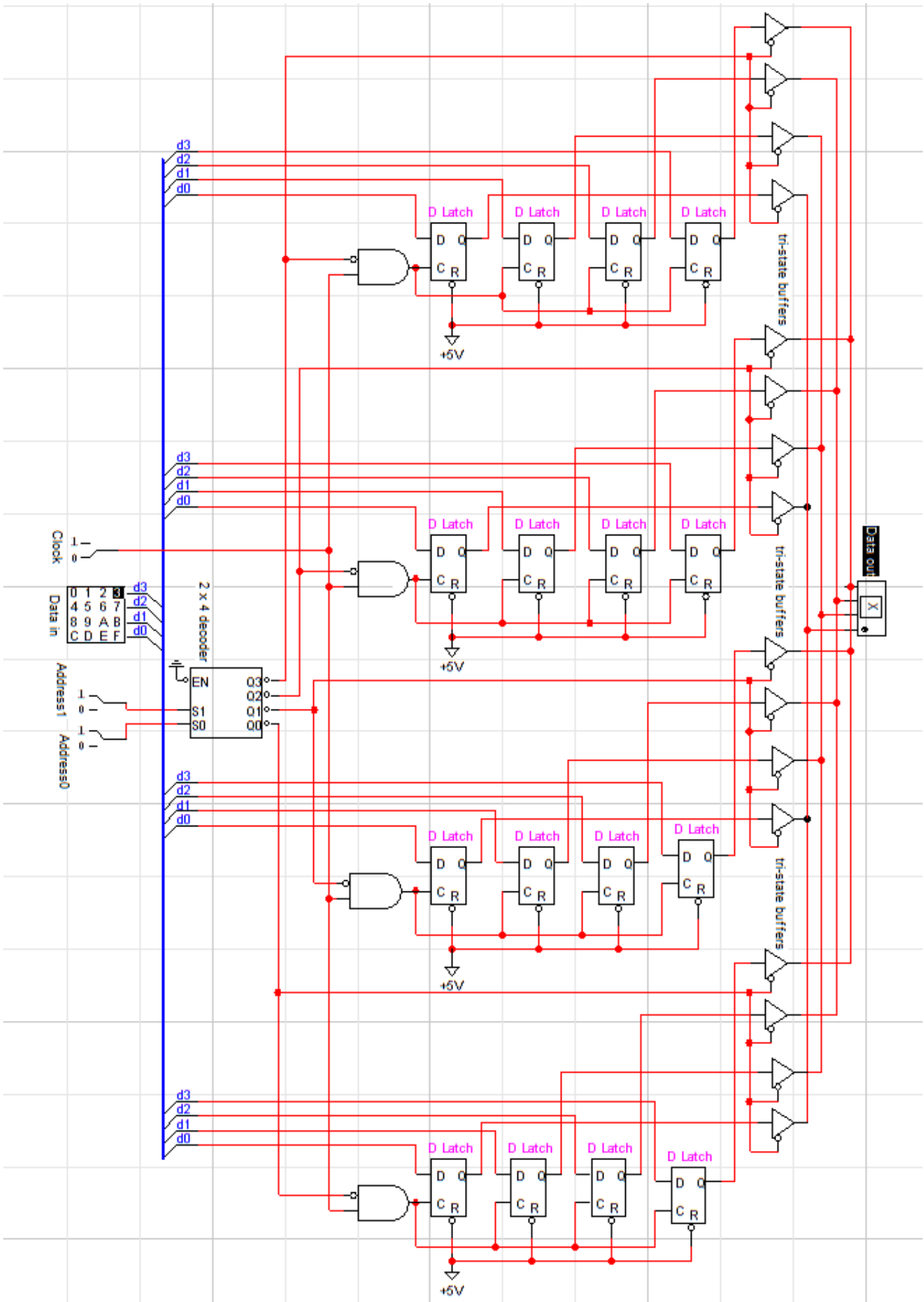
- **Write** is the write control signal.
- **Write register** is the number of a register to be written with a new value
- **Read register number 1** and **2** indicate which 2 registers can be read at data ports **Read data 1** and **Read data 2** at any given time
- clear and clock (**CLR** and **CLK**) are shared by all the 16 registers.
- **CLR** is active low



- 2 sets of 4 x 1 multiplexers select which 2 registers are currently being output at the two read ports.

- A decoder uses the write register number to select which of the 4 registers will receive a new value on a write.

RAM memory contains multiple flip-flops, organized into n-bit words, where each word can be accessed through use of an address


d3
d2
d1
d0
D Latch
D Q
C R
+5V
tri-state buffers
Clock
Data in
Address1
Address0
2 x 4 decoder
EN
S1
S0
Q3
Q2
Q1
Q0
Data out

Finite State Machines elevator problem from lab assignment and traffic signal