Reading. Patterson and Hennessy §4.1 -- §4.8

Exercise 9.1. Describe the effect that a single stuck-at-0 fault (i.e., regardless of what it should be, the signal is always 0) would have for the signals shown below, in the single-cycle datapath shown in Figure 4.17, on page 322 (Figure 5.17 on page 307 of the third edition) of the text. Which instructions, if any, will not work correctly? Explain why?

Consider each of the following faults separately:
   a. RegWrite = 0
   b. ALUOp0 = 0
   c. ALUOp1 = 0
   d. Branch = 0
   e. MemRead = 0
   f. MemWrite = 0

Exercise 9.2. Consider the single-cycle datapath found in Figure 4.17, on page 322 (Figure 5.17 on page 307 in the 3rd edition) of the text. A friend is proposing to modify this single-cycle datapath by eliminating the control signal MemtoReg. The multiplexor that has MemtoReg as an input will instead use either the ALUSrc or the MemRead control signal. Will your friend’s modification work? Can one of the two signals (MemRead and ALUSrc) substitute for the other? Explain.

Exercise 9.3. The concept of the “critical path,” the longest possible path in the machine, was introduced in Section 4.4 on page 329 (Section 5.4 on page 315 of the third edition). Based on your understanding of the single-cycle implementation, show which units can tolerate more delays (i.e., are not on the critical path), and which units can benefit from hardware optimization. Quantify your answers under the assumption that memory units require 200 picosecond (ps), the ALU and adders require 100ps, and the Register file (read or write) requires 50ps. Further assume that the multiplexors, control unit, PC accesses, sign extension unit, and wires have no delay.

Exercise 9.4. If the time for an ALU operation can be shortened by 25% (compared to the description in Figure 4.26 on page 333 (Figure 6.2 on page 373 of the third edition) of the text):
   a. Will it affect the speedup obtained from pipelining? If yes, by how much? Otherwise, why not?
   b. What if the ALU operation now takes 25% more time?

Exercise 9.5. A computer architect needs to design the pipeline of a new microprocessor. She has an example workload program core with $10^6$ instructions. Each instruction takes 100 ps to finish.
a. How long does it take to execute this program core on a nonpipelined processor?
b. The current state-of-the-are microprocessor has about 20 pipeline stages. Assume it is perfectly pipelined. How much speedup will it achieve compared to the nonpipelined processor?
c. Real pipelining isn’t perfect, since implementing pipelining introduces some overhead per pipeline stage. Will this overhead affect instruction latency, instruction throughput, or both?

Solutions.

Exercise 9.6. Using a drawing similar to Figure 4.29 on page 337 (Figure 6.5 on page 377 of the third edition) of the text, show the forwarding paths needed to execute the following four instructions:

```
add $3, $4, $6
sub $5, $3, $2
lw $7, 100($5)
add $8, $7, $2
```