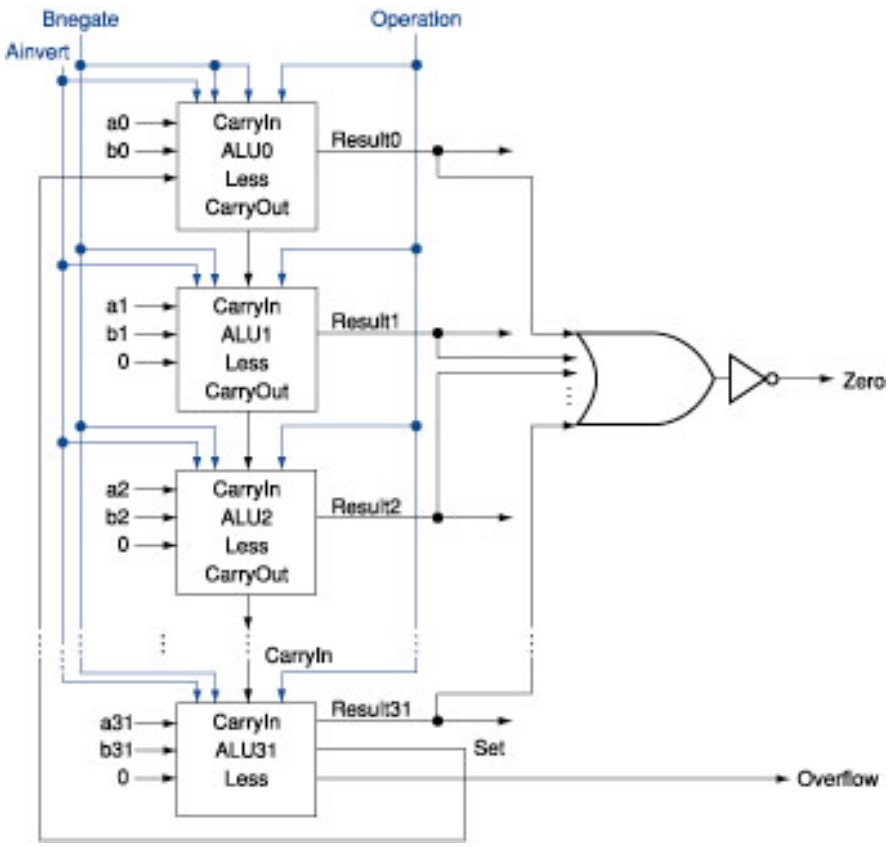
Computer Science 240
Assignment for Lab 7

NOTE: You should not try to do the problems on flip-flops until after lecture on Friday.

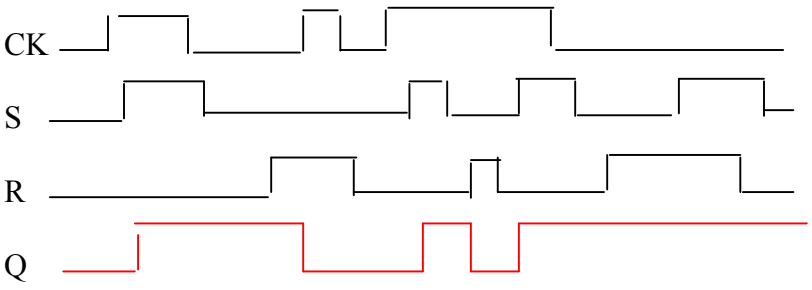
1. Given the following diagram for the ALU, and assuming A and B are 4-bit hexadecimal values, fill the table below:



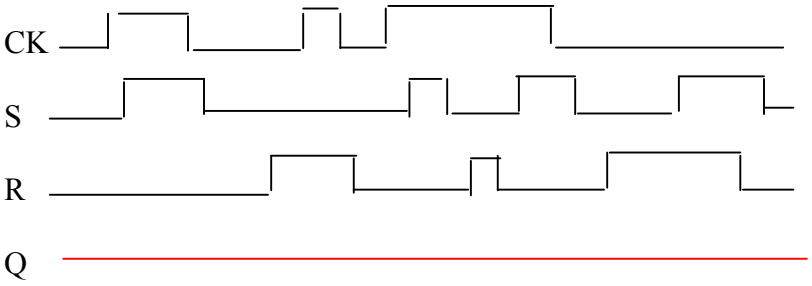
Function	Test Inputs	Output	Carry-out	Zero	Overflow
A + B	A = 3, B = 7	A	0	0	1
A + B	A = F, B =E	D	1	0	0
A AND B	A = 1,B = F	1	1	0	0
A AND B	A = 7, B = 8	0	0	1	0
A OR B	A = 3, B= C	F	0	0	0
A NOR B	A = 6, B= 9	0	1	1	0
SLT	A = 3, B= 9	0	0	1	1
SLT	A= C,B= 7	1	1	0	1

2. Assume you have an SR latch, S=0 and R=0. Do you know if the output Q is 0 or 1? Explain. You don't know, it could be either, depending on the previous state of the latch. The state of S = 0 R = 0 remembers the previous state.

3. Assume you have a clocked SR **latch**. Draw Q , given the following CK, S, and R:



4. Assume you have a clocked SR **flip-flop**, that is activated on the positive edge of the clock. Draw Q given the same CK, S, and R:



5. Explain why your outputs are different for the latch and the flip-flop:
The latch can change output whenever the CK signal is high. The flip-flop can only change output on the transition from low to high of the CK.