Memory Implementation

SRAM and DRAM

SRAMs and DRAMs

Small memories = register files.
(e.g., well, register sets!)

Medium-sized memories usually = SRAM (static random access memory)
(e.g., caches)

Large memories usually = DRAM (dynamic random access memory)
(e.g., main memory)

SRAMs

memory array, single access port
reasonably fast: slower than register file, faster than DRAM
**SRAM write** (time limits)

Setup, hold-time requirements for address + data.
Write-enable pulse of minimum width (not a clock edge).

**SRAM read port: data out**

Building a SRAM-sized register file is impractical.

A big enough output MUX has significant cascading gate delay.

Large memories use a shared output line, call a bit line.

No central gates/MUX to choose output!

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**Wired ORs** (don’t do this)

Danger, Will Robinson!

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**(noninverting) tristate buffers**

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SRAM write port:
data in

Organization of a 16 x 4 SRAM

Selecting location 1101

Another organization of a 16 x 4 SRAM

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Computer memory

But should we build a 12 to 2⁴ decoder?
Selecting location 0010

Nibbles "striped" across 4 smaller memories.

Selecting location 1101

Organization of a 4M x 8 SRAM

= 4 MB memory, size of a large cache for modern laptop

Dynamic RAM = DRAM

SRAM stores bit on pair of inverting gates:
- several transistors
- requires continuous (static) power.

DRAM stores bit as charge on capacitor:
- 1 transistor accesses stored charge.
- requires periodic refresh = read-write

In practice, single set of data lines often time-shared for read (out)/write (in).
FIGURE C.9.5 A single-transistor DRAM cell contains a capacitor that stores the cell contents and a transistor used to access the cell.

FIGURE C.9.6 A 4M × 1 DRAM is built with a 2048 × 2048 array. The row access uses 11 bits to select a row, which is then latched in 2048 1-bit latches. A multiplexor chooses the output bit from these 2048 latches. The RAS and CAS signals control whether the address lines are sent to the row decoder or column multiplexor.

Selecting bit number 101011*

Capture selected row in column latches

*Reminder: We wish to select bit number 101 011.

Meanwhile, dynamic bits are fading

*Reminder: We wish to select bit number 101 011.
Write back from column latches

3 to 8 row decoder

Mux

Dynamic bits are refreshed

Column latches

Maintain row bits during capture/hold

*Reminder: We wish to select bit number 101.011.

Finally, put bottom 3 address bits on address lines

3 to 8 row decoder

Mux

Double row decoder

Put bottom three bits onto shared address line 011

*Reminder: We wish to select bit number 101.011.

Disable row decoder