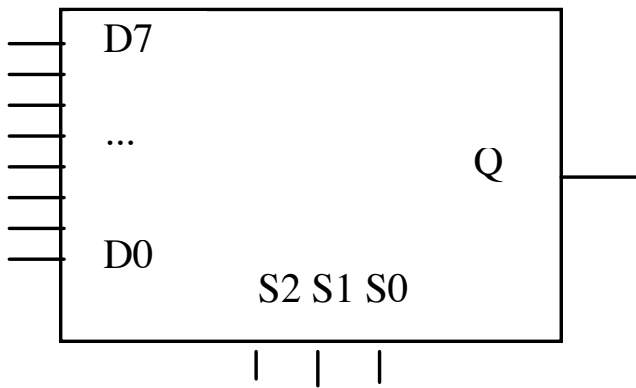# CS 240 Lab 3
Basic Digital Circuits

- **Multiplexer**

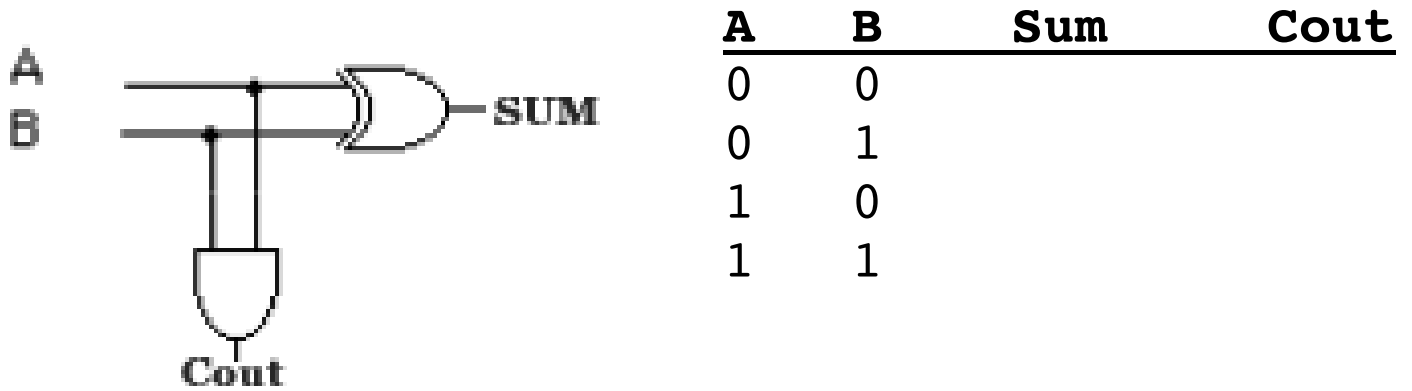- **Decoder**

- **Adder**

- **ALU**

Multiplexer
- n select lines
- 2^n input lines
- 1 output

One of the possible 2^n inputs is chosen by the n select lines, and gated through to the output of a multiplexer.

```
         ┌──────────────────┐
    ─────┤ D7               │
    ─────┤                  │
    ─────┤                  │
    ─────┤  ...          Q  ├─────
    ─────┤                  │
    ─────┤                  │
    ─────┤ D0               │
    ─────┤     S2 S1 S0     │
         └──────────────────┘
               │  │  │
```

S2	S1	S0	Q
0	0	0	D0
0	0	1	D1
0	1	0	D2
0	1	1	D3
1	0	0	D4
1	0	1	D5
1	1	0	D6
1	1	1	D7

Multiplexers are usually used for **selection**, but can also act as code detectors.

Decoder

      - n input/select lines

      - 2^n outputs

      - only one of the outputs is active at any given time, based on the value of the n select lines.

S2	S1	S0		Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
0	0	0	|	1	0	0	0	0	0	0	0
0	0	1	|	0	1	0	0	0	0	0	0
0	1	0	|	0	0	1	0	0	0	0	0
0	1	1	|	0	0	0	1	0	0	0	0
1	0	0	|	0	0	0	0	1	0	0	0
1	0	1	|	0	0	0	0	0	1	0	0
1	1	0	|	0	0	0	0	0	0	1	0
1	1	1	|	0	0	0	0	0	0	0	1

Half-Adder — adds two one-bit values

A	B	Sum	Cout
0	0		
0	1		
1	0		
1	1		

Full Adder — incorporates a carry-in
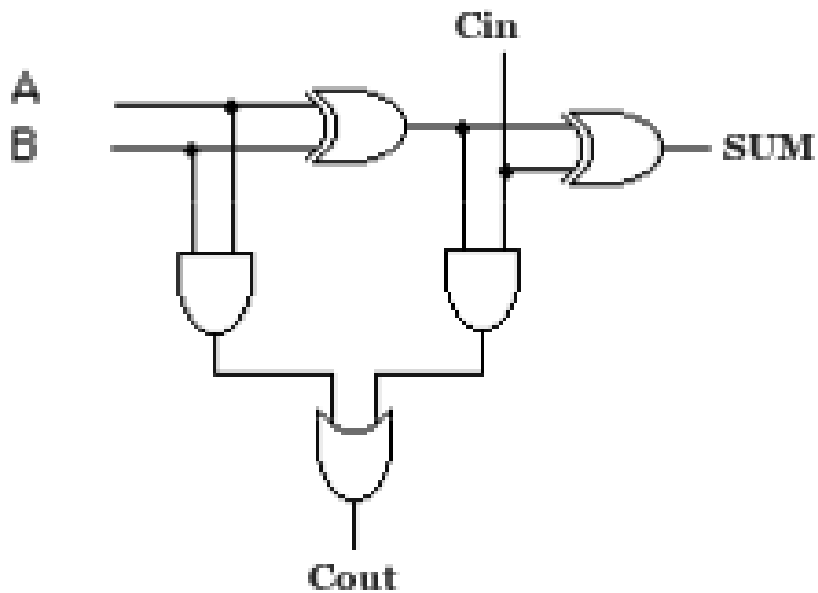
A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$Sum = A \oplus B \oplus Cin$

$Cout = AB + (A \oplus B)Cin$

n-bit adder = n 1-bit adders

Carry-out of each adder = Carry-in of the adder for next two most significant bits being added

ALU

Want to be able to select whether the ALU will produce the bitwise AND, OR, and sum as a result.
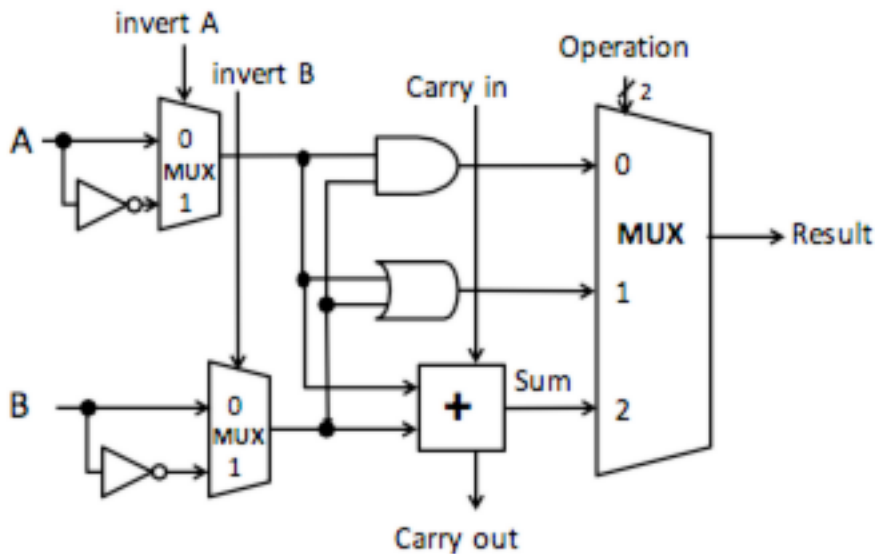
The basic operations and results are:

add $(a + b + Cin)$,

AND $(a \text{ AND } b)$,

OR $(a \text{ OR } b)$,

Adding the ability to choose whether to invert A or B provides additional operations:

sub $(\text{invert } b, Cin = 1, a + b + Cin)$

NOR (invert a, invert b, a AND b)

invA	invB	Cin	Op1	Op0	Result
0	0	X	0	0	a AND b
0	0	X	0	1	a OR b
0	0	0/1	1	0	a + b
0	1	1	1	0	a − b
1	1	X	0	0	a NOR b