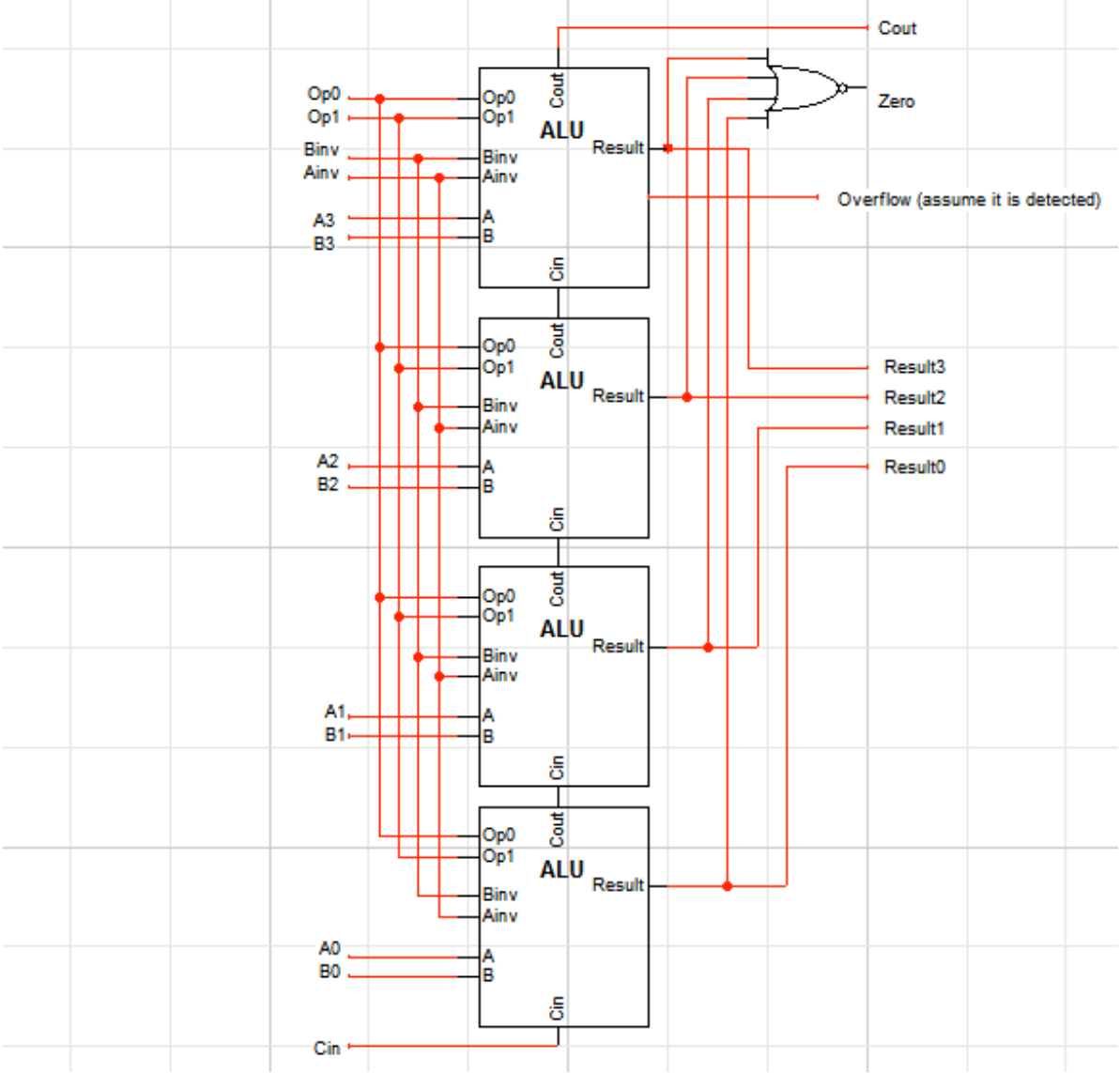
Computer Science 240
Memory and Data Path
Assignment for Lab 4

1. Given the following diagram for a 4-bit ALU, with A and B 4-bit hexadecimal values, complete the table below (assume that there is internal circuitry to detect overflow from an addition operation):



- Use ***4-bit, two's complement***, representation.
- Record **Result** as a ***hexadecimal value***; the other outputs are single bit (0 or 1).
- **Cout** and **overflow** come from adding **A** and **B**, even when the ALU function is a logical operation.

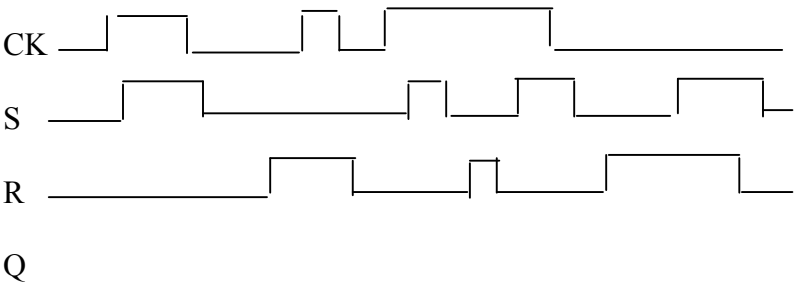
Function	Test Inputs	Result	Cout	Zero	Overflow
A + B	A = 3, B = 7	A	0	0	1
A + B	A = F, B =E				
A AND B	A = 1,B = F				
A AND B	A = 7, B = 8				
A OR B	A = 3, B= C				
A NOR B	A = 6, B= 9				
A - B	A = 3, B= 9				
A - B	A= C,B= 7				

2. Give the truth table and draw the circuit diagram for the SR latch:

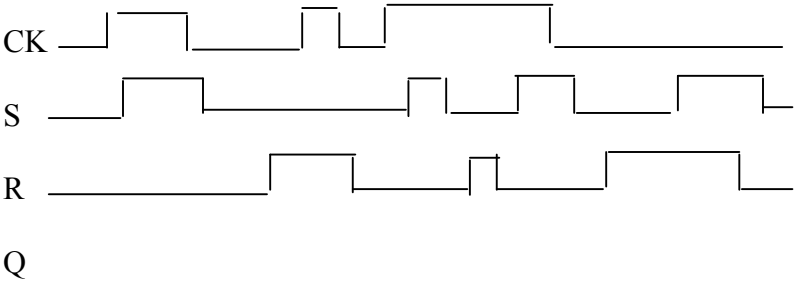
S	R	Q	Q'
0	0		
0	1		
1	0		
1	1		

3. Assume the inputs are S=0 and R=0. Do you know if the output Q is 0 or 1? Explain.

4. Assume you have a clocked SR **latch**. Draw Q , given the following CK, S, and R:



5. Assume you have a clocked SR **flip-flop**, that is activated on the positive edge of the clock. Draw Q given the same CK, S, and R:



6. Explain why the outputs are different for the latch and the flip-flop:

7. Review the notes from lecture on the HW ISA (an instruction set architecture for a small machine), and answer the following questions.

- How many instructions are there in the HW instruction set?

- How many bits are there in each instruction?

- What assembly language instruction is represented by the hexadecimal value 0x0021? (each digit represents 4 bits). Describe what you expect the instruction to do.

- What is the 16-bit binary form of the following instruction?

    ADD R1 R1 R4

- What are the contents of Register 1 and Register 4 after this instruction is executed?

- Given the following instruction stored at address 8 in memory:

    8: BEQ R5 R6 C

  Assume register 5 contains FFFE, and register 6 contains FFFE and that the offset is interpreted as a signed, 4-bit, two's complement values.

  After this instruction is executed, what will be the address of the next instruction?

- Repeat the previous question, but assume that the original value of register 5 = 0003, and register 6 = 0002. What will be the address of the next instruction?