

- b. Suppose the cache is **direct mapped** (but still with a capacity of 512 bytes for byte-addressable memory, using the same policies as in part a).
- i. If **A starts at 0x1000** and **B starts at 0x2000** (like in part a), what is the **miss** rate for the code above if the cache block size is
 1. **4** bytes?
 2. **8** bytes?
 3. **16** bytes?
 - ii. If **A starts at 0x1000** and **B starts at 0x1FF0**, what is the **miss** rate for the code above if the cache block size is
 1. **4** bytes?
 2. **8** bytes?
 3. **16** bytes?

2. Consider the following (partially blank) x86-64 assembly, (partially blank) C code, and memory listing. **Addresses and values are 64-bit**, and the machine is **little-endian**. All the values in memory are in hex, and the address of each cell is the sum of the row and column headers: for example, address 0x1019 contains the value 0x18.

<p>Assembly code:</p> <pre>foo: movl \$0, _____ L1: cmpq \$0x0, %rdi je L2 cmp _____, 0x1(%rdi) je _____ mov 0x8(%rdi), %rdi jmp _____ L2: ret L3: mov (%rdi), %eax jmp L2</pre>	<p>C code:</p> <pre>typedef struct person { char height; char age; struct person* next_person; } person; int foo(person* p) { int answer = _____; while (_____) { if (p->age == 24) { answer = p-> _____; break; } p = _____; } return answer; }</pre>
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Memory Listing
Bits not shown are 0.

	0x00	0x01	...	0x05	0x06	0x07
0x1000	80	1B	...	00	00	00
0x1008	80	1B	...	00	00	00
0x1010	3F	18	...	00	00	00
0x1018	3F	18	...	00	00	00
0x1020	00	00	...	00	00	00
0x1028	18	10	...	00	00	00
0x1030	18	10	...	00	00	00
0x1038	40	40	...	00	00	00
0x1040	40	40	...	00	00	00
0x1048	00	00	...	00	00	00

a. Complete the assembly and C code.

