CS 240 SI Worksheet
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Session #7
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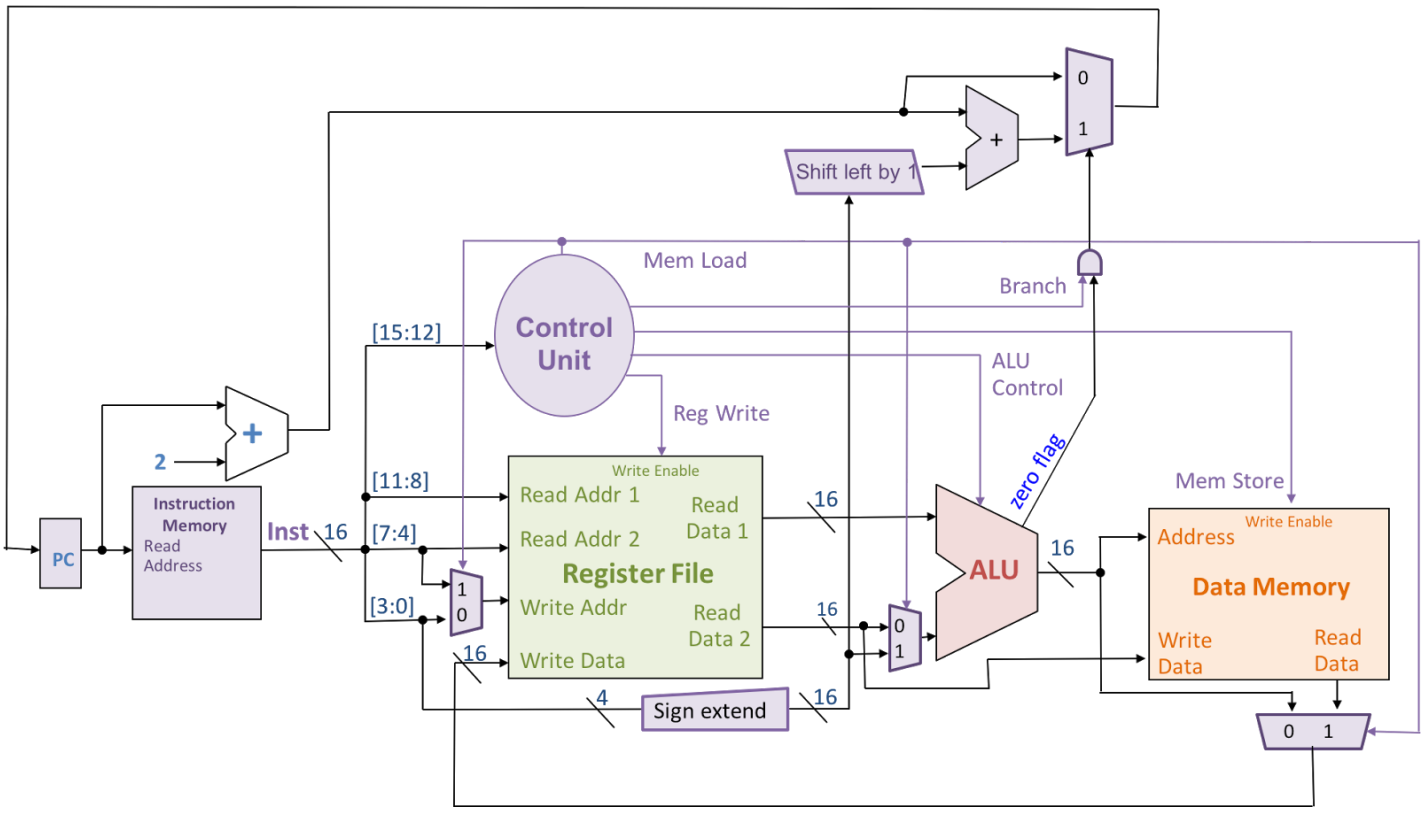
The Processor: Instruction Set Architecture + Microarchitecture

Complete the following table (only the blanks, not the ??):
(You get to simulate the program on the next page)

Address	Opcode	Operation	s	t	d/Offset
0x0 - 0x1		SUB	5	5	5
0x2 - 0x3		LW	6	7	4
0x4 - 0x5		BEQ	6	0	3
0x6 - 0x7		ADD	7	5	5
0x8 - 0x9		SUB	6	1	6
0xA - 0xB		BEQ	6	1	-4
0xC - 0xD		SW	6	5	4
0xE - 0xF	HALT				

Register File	
Reg	Contents
R5	??
R6	2
R7	??

Data Memory		
Address	Contents	
0x4 - 0x5	??	??
0x6 - 0x7	3	0



Given the state of the register file and data memory, **simulate each step** of the program and record the **state of the program counter, register file, and data memory after each step**, as well as the **outputs of the control unit** that enabled the execution of the instruction.

Instruction in Memory (in Assembly Syntax)	**PC**	**Reg File Changes**	**Data Memory Changes**	**ALU Control**	**Mem Load**	**Mem Store**	**Reg Write**	**Branch**