

Assignment for Lab 10
Cache Memory
Computer Science 240

NOTE: the assigned reading in the CSAPP text should be helpful in understanding how to solve these problems.

1. For each of the following independent assignments of bits in a **32-bit address** for use in a **direct-mapped cache**, answer the following questions.

	Tag	Index	Offset
A	31-10	9-4	3-0
B	31-12	11-5	4-0

- a. What is the cache line size in bytes?
 - b. How many entries does the cache have? (In other words, how many data lines/blocks can the cache store in total?)
 - c. What is the ratio between the total bits used by the cache over the bits required to store the data entries alone?
2. Starting from an empty cache, the following byte addresses are accessed in order (decimal notation is used): 0 4 16 132 232 160 1024 30 140 3100 180 2180

For *each* cache A and cache B:

- a. Show the final state of each *valid* entry in the cache by listing pairs of (index, tag) for each index in the cache.
- b. How many lines/blocks are misses (block needed is not in the cache)?
- c. How many cause a replacement in the cache (block needed maps to cache block in use with a different tag)?
- d. What is the hit rate (what percentage of accesses is the block needed already in the cache)?