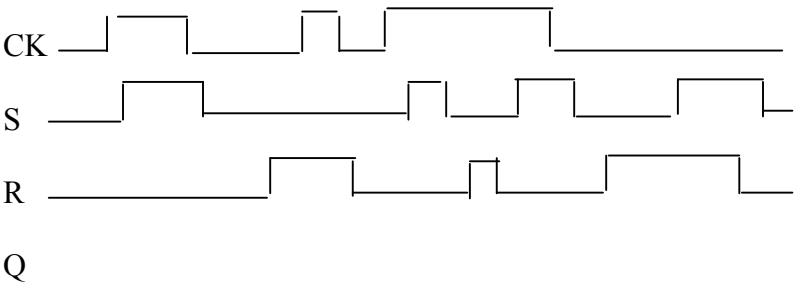
Computer Science 240
Memory and Data Path
Assignment for Lab 4

1. Give the truth table and draw the circuit diagram for the SR latch:

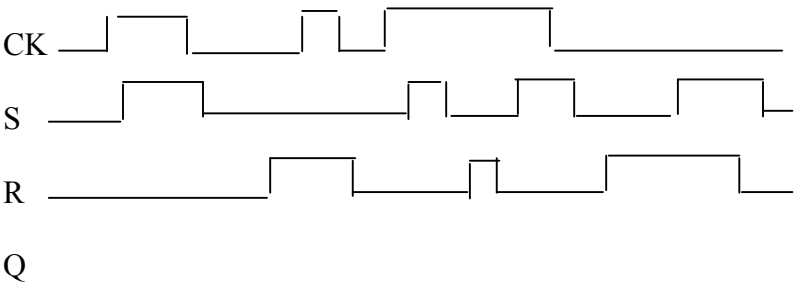
S	R	Q	Q'
0	0		
0	1		
1	0		
1	1		

2. Assume the inputs are S=0 and R=0. Do you know if the output Q is 0 or 1? Explain.

3. Assume you have a clocked SR **latch**. Draw Q , given the following CK, S, and R:



4. Assume you have a clocked SR **flip-flop**, that is activated on the positive edge of the clock. Draw Q given the same CK, S, and R:



5. Explain why the outputs are different for the latch and the flip-flop:

6. Review the notes from lecture on the HW ISA (an instruction set architecture for a small machine), and answer the following questions.

- How many instructions are there in the HW instruction set?

- How many bits are there in each instruction?

- What assembly language instruction is represented by the hexadecimal value 0x0021? (each digit represents 4 bits). Describe what you expect the instruction to do.

- What is the 16-bit binary form of the following instruction?

  ADD R1 R1 R4

- What are the contents of Register 1 and Register 4 after this instruction is executed?

- Given the following instruction stored at address 8 in memory:

  8: BEQ R5 R6 C

  Assume register 5 contains FFFE, and register 6 contains FFFE and that the offset is interpreted as a signed, 4-bit, two's complement values.

  After this instruction is executed, what will be the address of the next instruction?

- Repeat the previous question, but assume that the original value of register 5 = 0003, and register 6 = 0002. What will be the address of the next instruction?