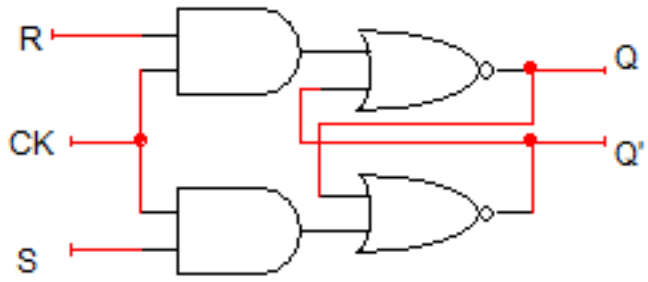
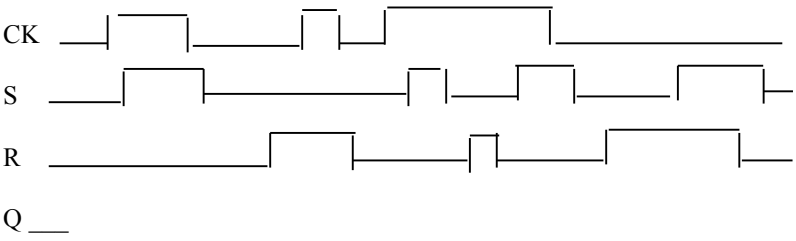
Computer Science 240
Memory
Assignment for Lab 4

1.Assume you are given a clocked SR latch:

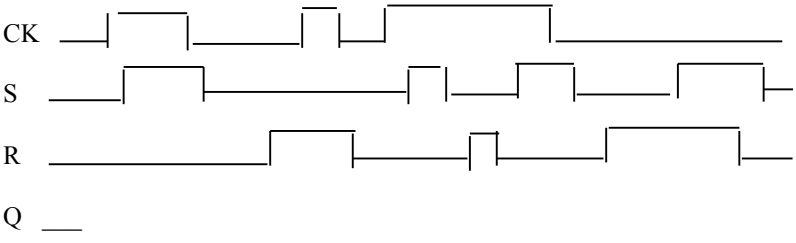


Draw Q assuming it is low initially, given the inputs shown for CK, S, and R:



2.Now, assume that you are instead given an SR flip-flop.

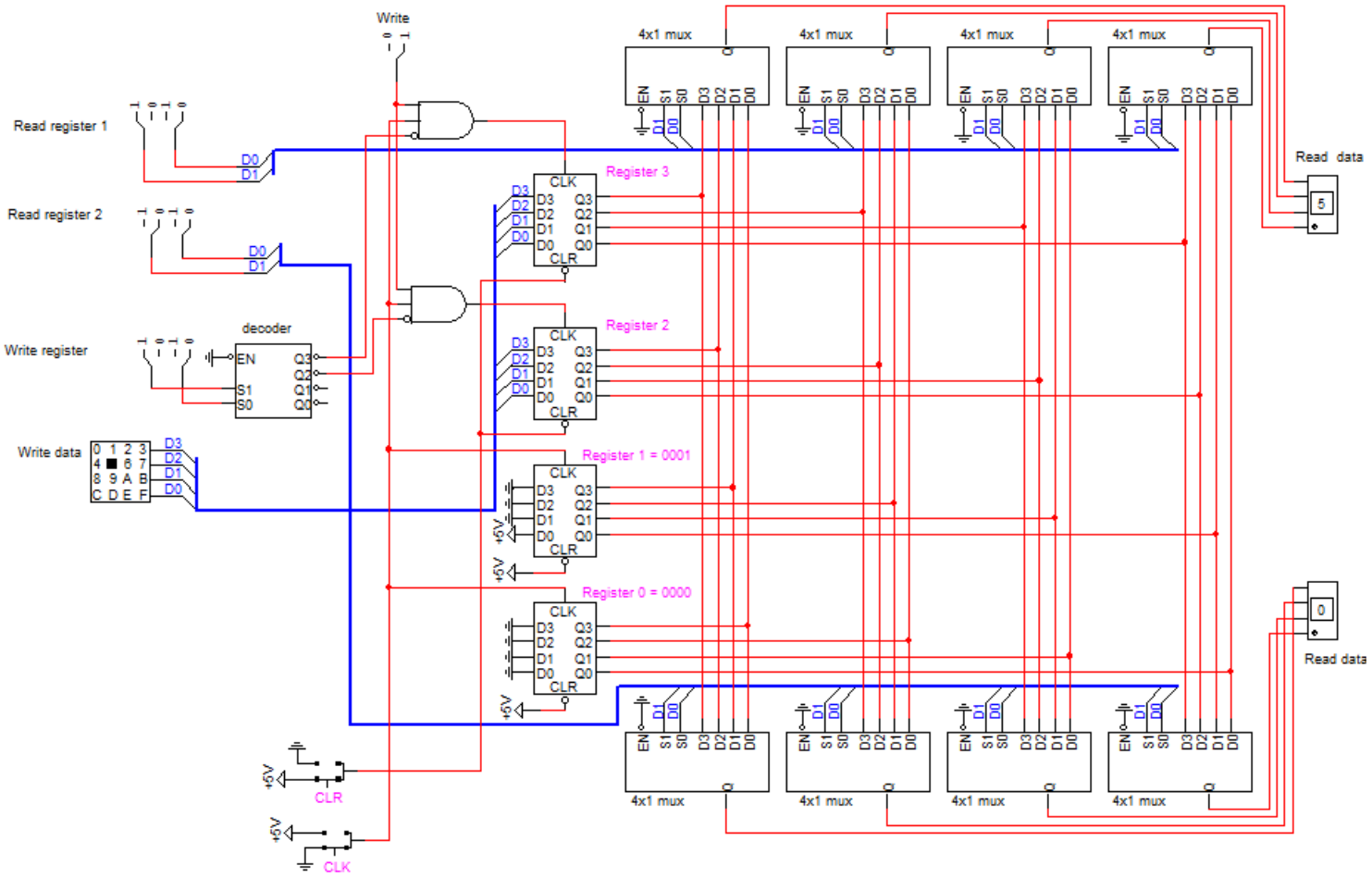
Draw Q assuming it is low initially, given the inputs shown for CK, S, and R:



3. Below is LogicWorks circuit which implements a register file for a set of 4 4-bit registers,

Register 0 always produces a value of 0, and register 1 always produces a value of 1 (those values are hardwired in this circuit).

This register file circuit is small enough that you can examine and understand the underlying circuitry:



4. What is the purpose of the decoder device in the circuit?

5. Explain how the multiplexers are used to produce the value of the specified registers and the Read data 1 and Read data 2 outputs: