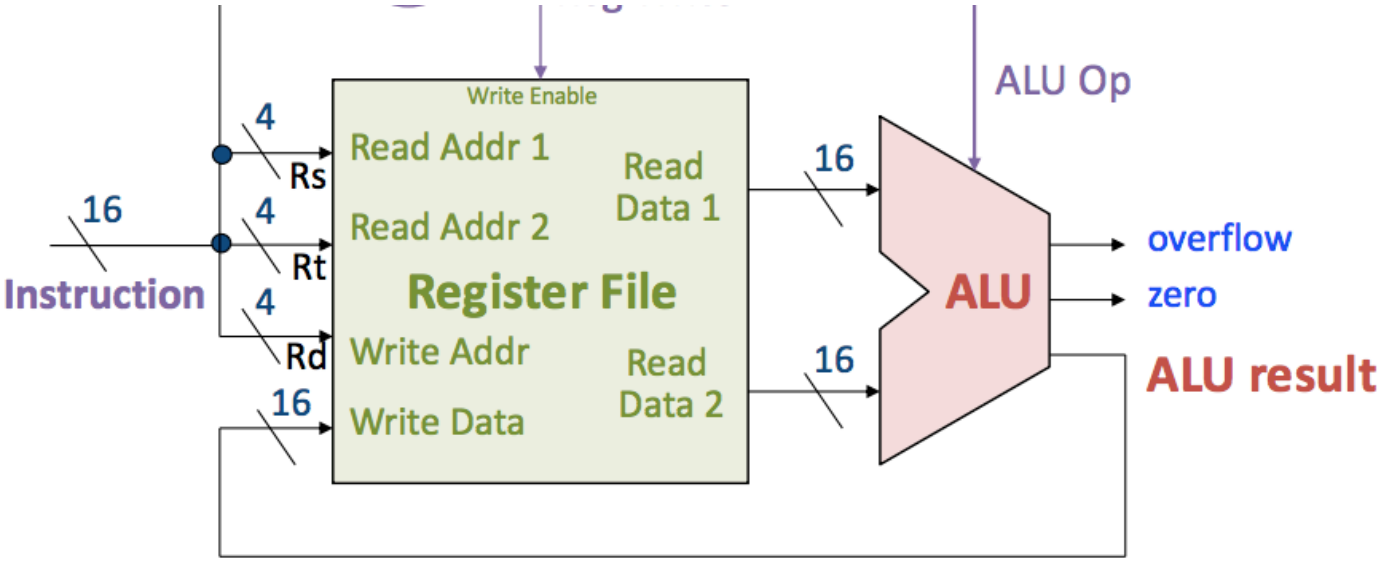
Assignment for Laboratory 5
Instruction Set Architecture
Computer Science 240

We ended lab last week with this concept of the CPU:



You will be spend part of the next lab implementing and experimenting with some of the CPU hardware needed to execute a set of instructions for a tiny computer.

We will call our tiny computer the HW computer. Here is a definition of some of the instructions for out computer (known as the Instruction Set Architeture, or ISA),

HW ISA Instructions

		16-bit Encoding (MSB … LSB)			
Assembly Syntax	**Meaning**	**Opcode**	**Rs**	**Rt**	**Rd**
ADD Rs, Rt, Rd	R[*d*] ← R[*s*] + R[*t*]	0010	*s*	*t*	*d*
SUB Rs, Rt, Rd	R[*d*] ← R[*s*] - R[*t*]	0011	*s*	*t*	*d*
AND Rs, Rt, Rd	R[*d*] ← R[*s*] & R[*t*]	0100	*s*	*t*	*d*
OR Rs, Rt, Rd	R[*d*] ← R[*s*] | R[*t*]	0101	*s*	*t*	*d*

Assume that the Rs, Rt, and Rd refer to the set of registers in the machine (R0 always contains a 0, R1 always a 1):

R: Register File

Reg	Contents	Reg	Contents
R0	0x0000	R8	
R1	0x0001	R9	
R2		R10	
R3		R11	
R4		R12	
R5		R13	
R6		R14	
R7		R15	

1. Assuming the opcode is 4 bits, how many instructions can be encoded in the HW instruction set (NOTE: it is more instructions that the 4 that are shown)?

2. How many bits are used to encode a register in an instruction?

3. What assembly language instruction is represented by the hexadecimal value 0x5012 (each digit represents 4 bits). Describe what you expect the instruction to do.

4. What is the 16-bit binary form of the following instruction?

ADD R1, R1, R4

5. What are the contents of Register 1 and Register 4 after this instruction is executed?