## Computer Science 240

 Combinational and Arithmetic LogicAssignment for Lab 3

1. Assume you have 3 inputs, $\mathbf{S}, \mathbf{A 1}$ and $\mathbf{A 0}$, and an output $\mathbf{Q}$.

When $\mathbf{S}=0, \mathbf{Q}=\mathbf{A 0}$
When $\mathbf{S}=1, \mathbf{Q}=\mathbf{A} \mathbf{1}$
Give the truth table for Q :

| $\mathbf{S}$ | $\mathbf{A 1}$ | $\mathbf{A 0}$ | $\mathbf{Q}$ |
| :--- | :--- | :--- | :--- |
| 0 | 0 | 0 |  |
| 0 | 0 | 1 |  |
| 0 | 1 | 0 |  |
| 0 | 1 | 1 |  |
| 1 | 0 | 0 |  |
| 1 | 0 | 1 |  |
| 1 | 1 | 0 |  |
| 1 | 1 | 1 |  |

Write a function for $\mathbf{Q}$, and simplify to a minimum number of gates:

Draw a circuit that produces $\mathbf{Q}$ :
$\mathbf{S}$ stands for "Select". Knowing this, describe in English what this circuit does:
2. Assume you have 2 inputs, A1 and A0, and 4 outputs/functions, Q0, Q1, Q2, and Q3

Q0 is only true when $\mathbf{A 1 A 0}=00$
Q1 is only true when $\mathbf{A 1 A 0}=01$
Q2 is only true when $\mathbf{A 1 A 0}=10$
Q3 is only true when $\mathbf{A 1 A 0}=11$

Give the truth table:

| A1 | A0 | Q0 | Q1 | Q2 | Q3 |
| :--- | :--- | :--- | :--- | :--- | :--- |
| 0 | 0 |  |  |  |  |
| 0 | 1 |  |  |  |  |
| 1 | 0 |  |  |  |  |
| 1 | 1 |  |  |  |  |

Write a function for each of $\mathbf{Q 0}, \mathbf{Q 1}, \mathbf{Q 2}$, and $\mathbf{Q 3}$ :
Q0 =
Q1 =
Q2 =
Q3 =

Draw a circuit that produces each of the functions from a single set of inputs A1 and A0:
3. Complete the truth table for two functions, Sum and CarryOut, which represent the result when adding two binary digits $\mathbf{A}$ and $\mathbf{B}$ :

| A | B | CarryOut | Sum |
| :--- | :--- | :--- | :--- |
| 0 | 0 |  |  |
| 0 | 1 |  |  |
| 1 | 0 |  |  |
| 1 | 1 |  |  |

Draw a circuit which produces Sum and CarryOut from inputs A and B (this circuit is know as a half adder). You should use exactly one AND gate and one XOR (exclusive or) gate.

Give the truth table for a full adder (which incorporates a carry-in bit to the sum of $\mathbf{A}$ and $\mathbf{B}$ ):

| A | B | CarryIn | CarryOut | Sum |
| :--- | :--- | :--- | :--- | :--- |
| 0 | 0 | 0 |  |  |
| 0 | 0 | 1 |  |  |
| 0 | 1 | 0 |  |  |
| 0 | 1 | 1 |  |  |
| 1 | 0 | 0 |  |  |
| 1 | 0 | 1 |  |  |
| 1 | 1 | 0 |  |  |
| 1 | 1 | 1 |  |  |

4. A circuit for the full adder is:


Circle the two half adders:

Explain what each half adder is doing, in relation to adding the three bits $\mathbf{A}, \mathbf{B}$, and $\mathbf{C i n}$ :

Explain what the OR gate is doing to produce the Cout:

