1. Complete the truth table for the following circuit (the box with **+** is a 1-bit adder):

Operation

Carry in

A

MUX → Result

B

Sum

+

Carry out
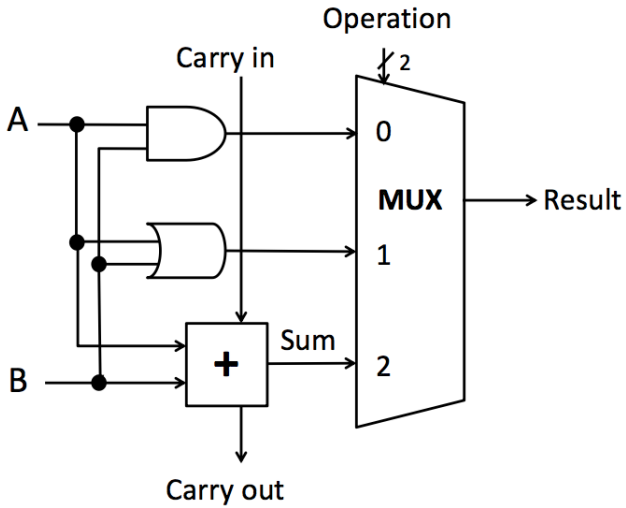
assume **Operation** is a 2-bit value **Op1 Op0**

Op1	Op0	Result (express in terms of A and B)
0	0	
0	1	
1	0	

Describe the general purpose of this circuit:

2. Complete the truth table for the SR latch:

3. Draw the circuit diagram for the SR latch:

S	R	Q	Q'
0	0		
0	1		
1	0		
1	1		

4. Assume the inputs are S=0 and R=0. Will the output Q be 0 or 1? Explain.