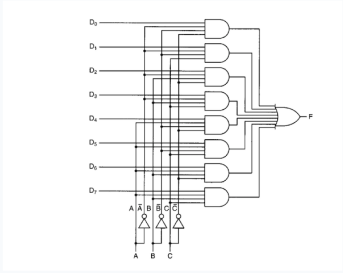
Warmup question from the reading: is the following a *decoder* or a *multiplexer*?



- Decoder
- Multiplexer (mux)
- None of the above

Start the presentation to see live content. For screen share software, share the entire screen. Get help at **pollev.com/app**

CS 240
Foundations of Computer Systems

WELLESLEY

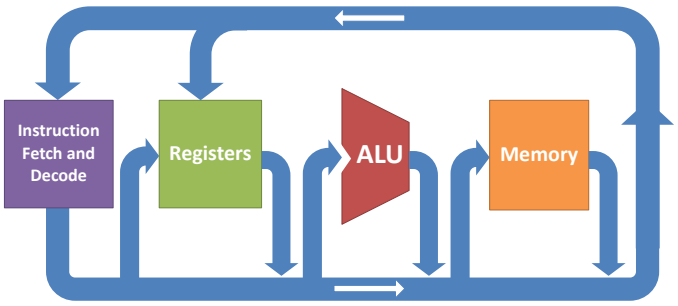
Combinational Logic

Building blocks: encoders, decoders, multiplexers

Abstraction!

https://cs.wellesley.edu/~cs240/

Goal for the next 2 weeks: **"Build" A Simple Processor**



Compiler/Interpreter

Operating System

ISA

Microarchitecture

Digital Logic

Devices (transistors, etc.)

Solid-State Physics

Toolbox: Building Blocks

Processor datapath

Instruction Decoder

Arithmetic Logic Unit

Adders
Multiplexers
Encoders
Decoders

Gates

Memory

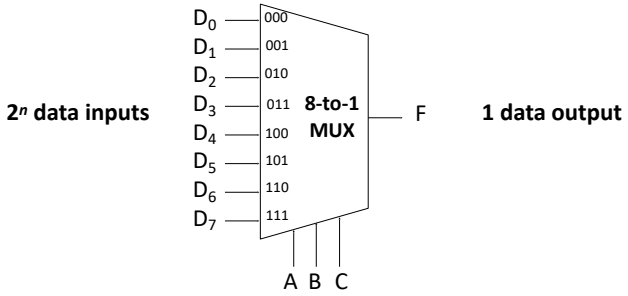
Registers

Flip-Flops
Latches

Abstraction!

Multi-bit Multiplexers

Select one of several inputs as output.



Multi-bit Multiplexers

Select one of several inputs as output.

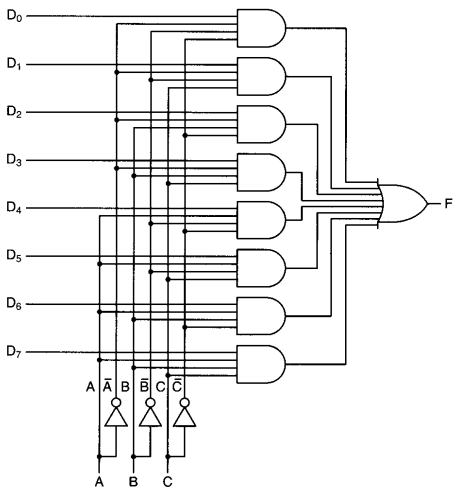
Example: selector lines ABC = 011 Output F = D_3

Multi-bit Multiplexers

Select one of several inputs as output.

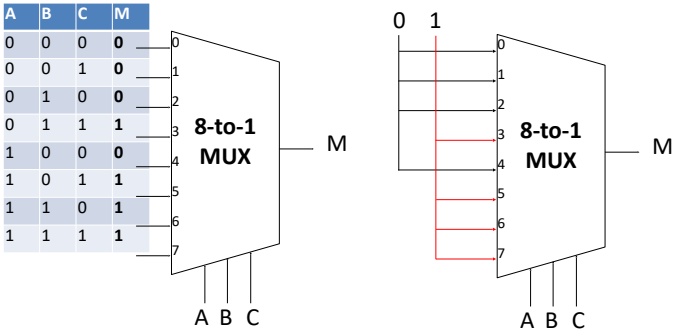
A MUX is conceptually an encoder (2^n inputs to n outputs) + selection

8-to-1 MUX with gates



MUX + voltage source = truth table

A	B	C	M
0	0	0	**0**
0	0	1	**0**
0	1	0	**0**
0	1	1	**1**
1	0	0	**0**
1	0	1	**1**
1	1	0	**1**
1	1	1	**1**

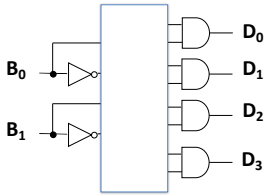


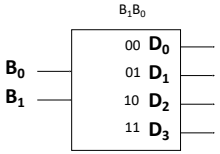
Decoders

ex

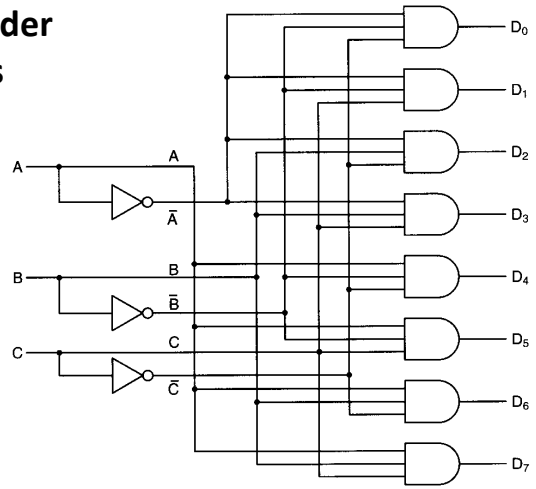
Decodes input number, asserts corresponding output.

- *n*-bit input (an unsigned number)
- 2^n outputs
- Built with code detectors.



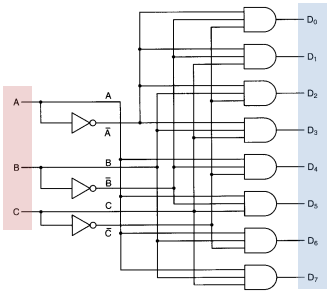


3-bit decoder with gates

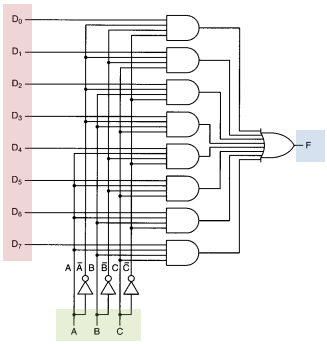


Decoders and multiplexers

A decoder has an n-bit input and 2^n outputs. Only 1 output active at once.



A multiplexer has 2^n inputs, n selector wires, and 1 output.



Buses and **Logic Arrays**

A bus is a collection of data lines treated as a single logical signal.
= *fixed-width value*

An array of logic elements (logical array) applies same operation to each bit in a bus.
= *bitwise operator*