Assignment for Lab 11

Computer Science 240

Adapted from P&H Exercise 5.4

For each of the following independent assignments of bits in a **32-bit address** for use in a **direct-mapped cache**, answer the following questions.

	Tag	**Index**	**Offset**
A	31-10	9-4	3-0
B	31-12	11-5	4-0

1. What is the cache line size in bytes?

2. How many entries does the cache have? (In other words, how many data lines/blocks can the cache store in total?)

3. What is the ratio between the total bits used by the cache over the bits required to store the data entries alone?

4. Starting from an empty cache, the following byte addresses are accessed in order (decimal notation is used): 0 4 16 132 232 160 1024 30 140 3100 180 2180

   a. Show the final state of each *valid* entry in the cache by listing pairs of (index, tag) for each index in the cache.

   b. How many lines/blocks are replaced during this sequence?

   c. What is the miss rate?