Computer Science 240 More Digital Logic

Assignment for Lab 3

1. Assume you have 3 inputs, S, A1 and A0, and an output Q.

When
$$S = 0$$
, $Q = A0$

When
$$S = 1$$
, $Q = A1$

Give the truth table for Q:

S	A1	A0	Q
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Write a function for Q, and simplify to a minimum number of gates:

Draw a circuit that produces Q:

S stands for "Select". Knowing this, describe in English what this circuit does:

2	Assume	you have 2 in	nuts A1	and AO	and 4 or	itnuts/functi	ions O	0 ()1	O^2	2 and	O_3
∠.	1 Issuille	you nave 2 m	puis, 111	and 110.	and \pm or	upats/ranet	ions, Q	υ, 、	<i>7</i> 1,	V	≥, anu	\mathbf{v}

Q0 is only true when A1A0 = 00Q1 is only true when A1A0 = 01Q2 is only true when A1A0 = 10

Q3 is only true when A1A0 = 11

Give the truth table:

A1	A0	Q0	Q1	Q2	Q3
0	0				_
0	1				
1	0				
1	1				

Write a function for each of Q0, Q1, Q2, and Q3:

Q0 =

Q1 =

Q2 =

Q3 =

Draw a circuit that produces each of the functions from a single set of inputs A1 and A0:

Each input combination of A1A0 represents a decimal number. How is this related to the outputs?

3. Complete the truth table for two functions, $Sum\$ and CarryOut, which represent the result when adding two binary digits A and B.

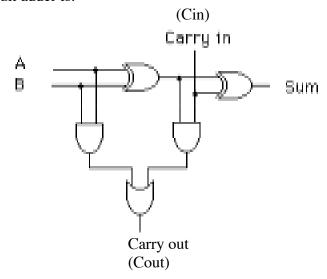
Α	В	CarryOut	Sum
0	0		
0	1		
1	0		
1	1		

Draw a circuit which produces Sum and CarryOut from inputs A and B (this circuit is know as a *half adder*). You should use exactly one AND gate and one XOR (exclusive or) gate.

Give the truth table for a *full adder* (which incorporates a carry-in bit to the sum of A and B):

A	В	CarryIn	CarryOut	Sum
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

A circuit for the full adder is:



Circle the two half adders.

Explain what each half adder is doing, in relation to adding the three bits A, B, and Cin:

Explain what the OR gate is doing to produce the Cout.