Assignment for Lab 11

Computer Science 240

1. For each of the following independent assignments of bits in a **32-bit address** for use in a **direct-mapped cache**, answer the following questions.

	Tag	Index	Offset
A	31-10	9-4	3-0
B	31-12	11-5	4-0

a. What is the cache line (block) size in bytes? Line size = 2^{offset} bytes

A: 16 bytes B. 32 bytes

b. How many entries does the cache have? (In other words, how many data lines/blocks can the cache store in total?) ? Cache size = 2^{index} entries

A: 64 blocks = B: 128 blocks

c. What is the ratio between the total bits used by the cache over the bits required to store the data entries alone? Total bits/Bits for data only = (Tag bits + valid bit + data bits)/data bits

A: (22 + 1 + 16x8)/16x8 = 1.18 B. (20 + 1 + 32X8)/32x8 = 1.08

2. Starting from an empty cache, the following byte addresses are accessed in order (decimal notation is used): 0 4 16 132 232 160 1024 30 140 3100 180 2180

a. Show the final state of each *valid* entry in the cache

A: (0,1) (1,3) (8,2) (10,0) (11,0) (14,0) B: (0,0) (4,0) (5,0) (7,0) (32,0) (68,0) (96,0)

b. How many misses?

A: 9 B: 7

c. How many lines/blocks are replaced?

A: 3 B: 0

d. What is the hit rate?

A: 3 hits/12 accesses = 25% B: 5 hits/12 accesses = 41.7%