

# 1. Basic combinational building blocks 2. Logic for arithmetic 

Common combinational circuits: encoders, decoders, multiplexers, adders, Arithmetic Logic Unit
(printed together, separate sets of slides online)

## But first...

## Recall: sum of products

logical sum (OR)
of products (AND)
of inputs or their complements (NOT).

| $A$ | $B$ | $C$ | $M$ |
| :--- | :--- | :--- | :--- |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

Construct with:

- 1 code detector per 1-valued output row
- 1 large OR of all code detector outputs

Is it minimal?

## Gray Codes = reflected binary codes

Alternate binary encoding designed for electromechanical switches and counting.

|  | 00 | 01 | 11 | 10 |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | 0 | 1 | 2 | 3 |  |  |  |
| 000 | 001 | 011 | 010 | 110 | 111 | 101 | 100 |
| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |

How many bits change when incrementing?

## Karnaugh Maps: find (minimal) sums of products

| gray code <br> order <br> $\boldsymbol{\psi}$ |  |  |  |  |  |  | $\mathbf{0 0}$ | $\mathbf{0 1}$ | $\mathbf{1 1}$ | $\mathbf{1 0}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathbf{0 0}$ | 0 | 0 | 0 | 0 |  |  |  |  |  |  |
| $\mathbf{A B}$ | $\mathbf{0 1}$ | 0 | 0 | 0 |  |  |  |  |  |  |
| $\mathbf{1 1}$ | 1 | 1 | 0 | 1 |  |  |  |  |  |  |
| $\mathbf{1 0}$ | 1 | 1 | 1 | 1 |  |  |  |  |  |  |

1. Cover exactly the 1 s by drawing a (minimum) number of maximally sized rectangles whose dimensions (in cells) are powers of 2. (They may overlap or wrap around!)
2. For each rectangle, make a product of the inputs (or complements) that are 1 for all cells in the rectangle. (minterms)
3. Take the sum of these products.

## Voting again with Karnaugh Maps

| A | B | C | M |
| :--- | :--- | :--- | :--- |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

## Goal for next 2 weeks: Simple Processor



## Toolbox: Building Blocks



## Microarchitecture

Processor datapath

Instruction Decoder
Arithmetic Logic Unit
Adders
Multiplexers
Demultiplexers
Encoders Decoders

Gates


Memory

Registers
Flip-Flops
Latches

## Decoders

Decodes input number, asserts corresponding output. $n$-bit input (an unsigned number) $2^{n}$ outputs
Built with code detectors.


## Multiplexers

Select one of several inputs as output.

$\boldsymbol{n}$ selector lines

## Build a 2-to-1 MUX from gates

If $S=0$, then $F=D_{0}$.
If $S=1$, then $F=D_{1}$.

1. Construct the truth table.

2. Build the circuit.


## MUX + voltage source = truth table



## Buses and Logic Arrays

A bus is a collection of data lines treated as a single logical signal.
= fixed-width value

Array of logic elements applies same operation to each bit in a bus.
= bitwise operator


