CS 240 Cache Divination - Paper Cache Name:

1. CSAPP 6.26

Cache	m	C	B	E	S	t	s	b
1								
2								
3								
4								

2. CSAPP 6.29

A.

Cache	Tag bits	Index bits	Offset bits

B.

Operation	Address	Hit?	Read Value

3. CSAPP 6.34

dst	Col 0	Col 1	Col 2	Col 3
Row 0				
Row 1				
Row 2				
Row 3				

src	Col 0	Col 1	Col 2	Col 3
Row 0				
Row 1				
Row 2				
Row 3				

4. CSAPP 6.36

A. Case 1: Assume the cache is 512-bytes, direct-mapped, with 16-byte cache blocks. What is the miss rate?

B. Case 2: What is the miss rate if we double the cache size to 1024 B?

C. Case 3: Now assume the cache is 512 bytes, 2-way set associative using an LRU replacement policy, with 16-byte cache blocks. What is the cache miss rate?

D. For Case 3, will a larger cache size reduce the miss rate?

E. For Case 3, will a larger block size help to reduce the miss rate?